Code :R7320206

III B.Tech II Semester(R07) Regular & Supplementary Examinations, April/May 2011
VLSI DESIGN
(Common to Electrical & Electronics Engineering, Electronics & Control Engineering, Electronics & Communication Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE questions
All questions carry equal marks

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1. What are the two advanced CMOS technologies and clearly explain about them.
2. (a) Explain about MOS gate capacitance model with the required diagrams.
   (b) MOS diffusion capacitance model with neat diagrams.
3. Design a stick diagram for NMOS EXNOR gate.
4. (a) What is a transmission gate? Explain clearly about it. Draw the symbols of transmission gate.
   (b) Implement XOR gate using transmission gate.
5. (a) What are standard cell libraries?
   (b) Discuss about the significance of standard cell libraries in implementation/ designing of chips.
6. (a) Write about standard cell based design.
   (b) Implement an optimized 3X8 binary decoder using PLA.
7. What is meant by simulation? Explain in detail about switch level and circuit level simulation.
8. What are test vectors? Explain with an example how PODEM algorithm is used for automatic generation of the test vectors.

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1. Clearly explain all types of fabrication of resistors and capacitors.
2. Mention different non ideal I-V effects and clearly explain about them.
3. Explain clearly about the limitations of scaling.
4. Implement 2:1 mux and 1:2 demux circuits using transmission gate.
5. Compare different techniques used to improve the addition time in adders as a trade-off with complexity and performance.
6. (a) Depending on principle of programming categorize the PLDs used to implement the System design.
   (b) Implement a full adder using PLA.
7. Summarize in detail the wide variety of simulators used at different levels of design abstraction.
8. (a) With the help of an example explain how physical defects are categorized as logical faults.
   (b) Explain the terms Controllability and Observability.

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Code :R7320206 **3**

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1. (a) Explain the fabrication process for a resistor.
   (b) Draw a lay out of a resistor.
2. (a) Explain the Tunneling mechanism in MOS devices.
   (b) How does the transistor characteristics are influenced by the temperature?
3. Tabularize the effect of scaling. Write about substrate doping.
4. Estimate the total delay when a larger load capacitance is driven by a large inverter gate N which is driven by a small gate N-1 and so on.
5. (a) Implement a full adder circuit using Transmission gates.
   (b) Construct an 8-bit Carry select adder Using adders and multiplexers.
6. Give the significance of standard cell library in optimizing the design of a chip? Categorize various modules available in the library according to size.
7. Write a program in VHDL for an 8:1 multiplexer in behavioral and structural style and compare them.
8. (a) What is meant by fault simulation? Explain.
   (b) Compare Serial fault simulation and parallel fault simulation.

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1. What are the four major CMOS technologies? Explain any one with flow chart.
2. Draw the circuit of a CMOS inverter. Draw and explain its DC characteristics.
3. Design a stick diagram for two input PMOS NAND and NOR gates.
4. What are the main sources of delay through a single gate? Mention the two possible solutions for that delay and explain them with a neat diagram.
5. Compare carry select, carry skip and carry look ahead adders with respect to speed, area and computing cost.
6. (a) Explain about the designing of a chip with sea of gates(SOG).
   (b) Write about FPGA.
7. (a) Discriminate between logic level simulation and Switch level simulation.
   (b) Write about Behavioral Synthesis.
8. Discuss in detail about the Boundary Scan architecture and its principle of testing the ICs at board level.

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